

USB-2XT -- USB PROBING SUPPORT PRODUCT

For Use With Tektronix® Logic Analyzers



USB-2XT Hardware Features

- Highest-performance USB2.0/1.1/1.0 probing available, with three performance-enhancing options available
- Supports probing a first USB channel with high-speed (HS), full-speed (FS) or low-speed (LS) bus traffic
- Optionally supports probing a second high-speed (HS) USB channel, using same or second analyzer acquisition module
- Front-end circuitry features non-repeater probing connection, with minimal high-speed signal distortion achieved via ultra-short on-board USB signal path
- Acquires and displays all aspects of bus behavior, including: USB On-The-Go (OTG) sequences; chirp speed negotiation; suspend, resume, and other bus events; packets; transactions; control transfers with device class decoding
- Seamless tracking of bus activity across HS and FS/LS domains
- Optionally tracks bus utilization, and optionally reports error statistics on address or endpoint basis
- Produces one or two 34-channel sets of bus data for analyzer acquisition; optionally produces 68-channel data
- Works with Tektronix® TLA5xxx/6xx/7xx/7xxx logic analyzers with 34-channel minimum (68-channel recommended) 60-MHz acquisition modules (120 MHz acquisition rate for specific configurations), and high-density P6434 (Mictor®) probes (P6860-type probes are supported with the use of Tektronix 020-2457-00 adapters; P69xx (D-Max) probes are supported with the use of Nexus Technology NEX-HDSWIZP69 adapters)
- Highly-efficient use of acquisition memory: just two samples needed for most bus events and packets, with data packets averaging three bytes per sample (for 34-channel acquisition; 2x further improvement for 68 channels)
- Powered via rear-panel USB2.0 (full speed) connection; module configuration/control via supplied control application
- Application control of target Vbus connection, facilitating re-enumeration without unplugging cables
- Application control of selective acquisition of PRE and/or SOF bus packets
- Application control of selective acquisition of Chirp, EOP and/or Idle bus events
- Application control of selective acquisition of number of data packet data bytes, 2-1024 bytes specifiable
- Application control of marking for selective acquisition of any or all of twenty-two (22) different types of transactions (including In-NAK, Out-NAK, Ping-NAK and Ping-ACK)
- Supplementary decoding of packet activity into byte-wide streaming data, facilitating serial-data-triggering applications
- Packet and event duration tracking performed by hardware, independent of logic analyzer timestamping
- Numerous packet and event error types can be detected and triggered on
- In-the-field firmware upgrading supported via the control application
- Compact form factor 5" x 4.2" x 1.3" (12,7cm x 10,7cm x 3,3cm) extruded-aluminum case

Software Features

- Graphical user interface support for complex multi-state logic analyzer trigger programs
- Powerful debug capabilities for triggering on and/or selective storage of events, packets and transactions
- Trigger on and/or selective acquisition of real-time bus anomalies as well as normal bus behavior
- Optionally trigger on packet byte-wide streaming data
- Logic analyzer system software inherently supports time-coordinated display of multiple listing and waveform windows, along with window-linked cursor control
- System software has multiple display modes for analyzer-acquired timestamp information with up to 125 ps timing resolution (time from prior-displayed event, from system trigger occurrence, or absolute time)
- Listing window high-level hierarchical display shows bus events and packets, transactions or control transfers, the latter with device class decoding
- Logic analyzer system software provides extensive facilities to search listing and waveform windows for text or data information of interest
- Optionally supports continually-updated histogram display of continuously-acquired bus utilization statistics
- Listing display controls affecting error, radix, control transfer details, event/packet duration, packet speed, packet direction and packet locality displays are provided
- Address-endpoint-based selective display controls provided (address-endpoint, mask, direction)
- Split-transaction-related selective display controls provided (hub address, hub address mask, hub port, hubport mask, endpoint type)
- Controls provided to enable/disable display of transactions based on the packet types present or absent in the transaction
- Controls allow suppression of display of trailing data bytes of lengthy data packets, complementing the hardware-implemented selective storage facility which can suppress the storage of such data bytes
- Controls provided to suppress display of specified types of acquired bus events
- System software supports multiple acquisition modules, allowing time-coordinated probing and display of USB activity along with e.g. that of the USB device- or USB host-processor, with high-level source code language display supported
- Many acquisition-related controls and selections are provided
- A plethora of display controls and display-related selections exist; numerous specific errors can be reported on
- Off-line viewing of acquisitions using any Windows system, with no logic analyzer required

USB-2XT Ordering Summary

- Includes USB-2XT probe adapter, USB cables, and CDROM with documentation, software and related files
- Part number USB-2XT-1 denotes the basic USB-2XT unit, probing HS/FS/LS traffic on one USB channel using 34-channel logic analyzer acquisition, to which any or all of the following performance-enhancing options can be added:
- Option USB-2XT-2 adds 68-channel logic analyzer acquisition capability (provides 2x more-efficient use of acquisition memory, and facilitates complex trigger constructs)
- Option USB-2XT-4 adds statistics-tracking and bus-monitoring capabilities (statistics capability allows acquisition of and triggering on long-term bus utilization and error occurrence summary information (HS/FS traffic only)); monitor capability provides real-time application display of bus event and packet activity, and Vbus-power voltage and current readings, including minimum and maximum values, independent of logic analyzer acquisitions, and (for HS traffic only, when using 68-channel acquisition (requires USB-2XT-2 option)) acquisition of and triggering on Vbus readings
- Option USB-2XT-8 option adds second USB channel capability (HS traffic only) (two-channel triggering and acquisition can utilize two independent 34-channel acquisition modules, else a single 68-channel acquisition module (requires USB-2XT-2 option) with output multiplexing of both channels' data)
- USB-2XT part numbers are formed by summing desired options; USB-2XT-1 through USB-2XT-15 are valid part numbers
- USB-2XT units can be shipped with desired options enabled, or options can be purchased later and enabled in the field

Contact Crescent Heart Software

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- Crescent Heart Software, a Tektronix® Embedded Systems Tools Partner and a member of the Tektronix® Logic Analyzer Third Party Developer team, is headquartered in Portland, Oregon USA.
- Crescent Heart Software has been a member of the USB Implementer's Forum (USB-IF), and has provided technical consultation and feedback regarding electrical signaling issues to the Version 1.1 and 2.0 USB specification definers.
- Information presented herein is subject to change without notice (datasheet Rev. F, September 2008)