

USB-2XP INDUSTRIAL-STRENGTH USB PROBING

For Use With Tektronix® Logic Analyzers



USB-2XP shown with case open and high-density Mictor® probes attached

USB-2XP Hardware Features

- Highest-performance USB2.0/1.1/1.0 probing available in three cost/performance models
- Probes high-speed (HS), full-speed (FS) and low-speed (LS) bus traffic, including USB OTG sequences
- Proprietary high-performance front-end circuitry with non-repeater probing connection
- Minimal high-speed signal distortion achieved via ultra-short USB signal path (0.35" (8,9 mm))
- Acquires and displays low-level HS/FS/LS bus signaling, with bit-, field- and packet-level annotation
- High-speed signaling timing resolution of 694 ps (1.44 GHz (3x oversampling) rate)
- Acquires and displays all aspects of bus behavior, including: low-level signaling; chirp speed negotiation; suspend, resume, other bus events; packets; transactions; control transfers with device class decoding
- Seamless tracking of bus activity across USB2.0 and USB1.1/1.0 domains
- Ten LEDs provide visual indication of Vbus, Reset, Idle, Packet-from-host, Packet-to-host, Speed, Suspend, Error and other activities (continuously functional)
- Continuously tracks bus utilization, error statistics on address or endpoint basis, continually reportable
- Works with Tektronix® TLA5xxx/6xx/7xx/7xxx logic analyzers with 34-channel minimum (68-channel recommended) 100 MHz acquisition modules, high-density Mictor® probes (recommended) or standard probes, compression probes supported with use of "Mictor-on-the-PCB" adapters
- Highly-efficient use of acquisition memory: two samples used for most bus events and packets, with data packets averaging three bytes per sample (for 34-channel acquisition; 2x improvement for 68 channels)
- Supports simultaneous connection of multiple acquisition modules
- Toggle switch controlled Vbus disconnection facilitates re-enumeration without unplugging cables
- Dip switch controlled selections optionally suppress acquisition of PRE and/or SOF bus packets
- Dip switch controlled selections optionally suppress acquisition of Chirp, EOP and/or Idle bus events
- Dip switch controlled selections optionally suppress acquisition of data bytes, 2-1024 bytes specifiable
- Dip switch controlled selections optionally mark and/or suppress acquisition of any or all of 22 different types of transactions (including In-NAK, Out-NAK, Ping-NAK and Ping-ACK)
- Decoding of packet activity into byte-wide streaming data to further facilitate triggering
- Packet and event duration tracking performed by hardware, independent of logic analyzer timestamping
- Probe adapter detects seven packet errors and twenty-four event errors, which can be triggered on
- Test point access to monitor buffered versions of D+ and D- signals and USB transceiver X+, X- and XDiff outputs
- Test point access to monitor Vbus voltage and current (via 0.1 Ohm sensing-resistor voltage drop)
- Test point access to monitor Vbus current, as output of wideband current-to-voltage amplifier with jumper-selectable gain of X1 to X100, permitting measurements of Vbus inrush current, connect current, operating current and suspend current when using a digital multimeter or DSO
- Test point access to monitor occurrence of SOF packets
- Test point access to monitor high-speed D+/D- differential analog waveform, disconnect signal output
- Test point access to monitor normal-, chirp- and disconnect-level HS thresholds, thresholds are adjustable

Software Features

- Graphical user interface support for complex multi-state logic analyzer trigger programs
- Powerful debug capabilities for triggering on and/or selective storage of events, packets and transactions
- Trigger on and/or selective acquisition of real-time bus anomalies as well as normal bus behavior
- Optionally trigger on packet byte-wide streaming data
- System software inherently supports time-coordinated display of multiple listing and waveform windows, along with window-linked cursor control
- System software has multiple display modes for analyzer-acquired timestamp information with 500 ps timing resolution (time from prior-displayed event, from system trigger occurrence, or absolute time)
- Listing window high-level hierarchical display shows bus events and packets, transactions or control transfers, the latter with device class decoding
- Low-level waveform display of bus activity can be viewed via a waveform window (for full- and low-speed traffic) or in a listing window (for high-speed traffic)
- Logic analyzer system software provides facilities to search listing and waveform windows for text or data information of interest
- Supports continually-updated histogram display of continuously-acquired bus utilization statistics (model USB-2XP-C)
- Listing display controls affecting error, radix, control transfer details, event/packet duration, packet speed, packet direction and packet locality displays are provided
- Address-endpoint-based selective display controls provided (address-endpoint, mask, direction)
- Split-transaction-related selective display controls provided (hub address, hub address mask, hub port, hubport mask, endpoint type)
- Controls provided to enable/disable display of transactions based on the packet types present or absent in the transaction
- Controls allow suppression of display of trailing data bytes of lengthy data packets, complementing the hardware-implemented selective storage facility which can suppress the storage of such data bytes
- Controls provided to suppress display of specified types of acquired bus events
- System software supports multiple acquisition modules, allowing time-coordinated probing and display of USB activity along with e.g. that of the USB device- or USB host-processor, with high-level source code language display supported
- Six acquisition controls with fifteen total acquisition-related selections
- Eighty-two display controls with two hundred twenty-two display-related selections
- Well over one hundred specific errors can be reported on
- Tektronix® TLA application allows off-line viewing on any Windows system, with no logic analyzer required

USB-2XP Ordering Summary

- Includes USB-2XP probe adapter, power supply, USB cables, AC power cord and software
- Model USB-2XP-A probes HS/FS/LS traffic using 34-channel acquisition
- Model USB-2XP-B additionally supports 68-channel acquisition, use of which provides for: 2x more efficient use of acquisition memory; facilitation of complex trigger constructs; optional acquisition and annotated display of low-level FS/LS bus behavior (sampled at 60 MHz)
- Model USB-2XP-C additionally provides support when using 68 channel acquisition for: optional acquisition and annotated display of low-level HS bus behavior (sampled at 1.44 Ghz); continuous tracking and optional continual reporting of bus utilization and error statistics

Contact Crescent Heart Software

- Internet: www.c-h-s.com; E-mail: sales@c-h-s.com; Voice: (+1)503-232-2232; Facsimile: (+1)503-232-2255
- Crescent Heart Software, a Tektronix® Embedded Systems Tools Partner and a member of the Tektronix® Logic Analyzer Third Party Developer team, is headquartered in Portland, Oregon USA.
- Crescent Heart Software has been a member of the USB Implementer's Forum (USB-IF), and has provided technical consultation and feedback regarding electrical signaling issues to the Version 1.1 and 2.0 USB specification definers.
- Information presented herein is subject to change without notice (datasheet Rev. Q, September 2006)