CRESCENT HEART SOFTWARE

SATA-6G
PROBE ADAPTER AND SOFTWARE

FOR USE WITH
TEKTRONIX TLA5XXX/6XX/7XX/7XXX
LOGIC ANALYZERS

USERS' MANUAL

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Please communicate suggestions for product and documentation improvements to **tech_support@c-h-s.com.**

Notice Regarding TLA Probes' Connection/Disconnection

In protocol analysis applications, it is critical that logic analyzer probes be connected and disconnected from the SATA-6G only when the unit is **not** powered on.

Refer to Section 1.2.1.2 of this document for further information in this regard.

Notice Regarding TLA Version 5.x System Software Issues

In protocol analysis applications, known issues exist involving TLA System Software Version 5.x (and possibly other Versions as well), such that Disassembly Properties display controls having numeric values and which are intended to have non-zero default values, are improperly initialized to zero.

For the SATA6GA disassembler, the affected controls are:

- **Maximum Num Data** (refer to Section 4.1.4.29)
- **Max Data Display Lines** (refer to Section 4.1.4.31)

The result of these controls having unintended default values of zero is that display of frame data information may be unintentionally suppressed, or display of entire frames may be unintentionally suppressed.

The workaround is to set the controls to non-zero values as appropriate. Each control can be set to its intended default value, which is 99,999,999; alternatively other, smaller values can be used, as desired.

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1. INTRODUCTION

This manual describes the setup and use of the SATA-6G probe adapter and companion software for protocol analysis of Serial ATA subsystems with datarates of 1.5 Gb/s, 3 Gb/s or 6 Gb/s using Tektronix TLA5xxx/6xx/7xx/7xxx logic analyzers (TLAs), as well as setup and use for frame error rate (FER) and bit error rate (BER) testing without use of a TLA logic analyzer.

This is an **advance version** of the SATA-6G product documentation, providing information that relates largely to the differences between the SATA-6G and the preceding SATA-II product. This document (together with the forward-looking SATA-6G datasheet) and the detailed SATA-II Users' Manual constitute the currently-available SATA-6G documentation, until such later time as an in-depth, formal SATA-6G Users' Manual document is made available.

Skimming, reading and/or studying the formal SATA-II Users' Manual is required in order to be able to understand the successor SATA-6G product functionality. This document can be skimmed before so doing, but should be read or studied again once the SATA-II product information has been well understood.

1.1 GENERALLY-RELEVANT INFORMATION

1.1.1 Similarity With The SATA-II

It should be understood that the SATA-6G hardware and software function and behave 95%+ the same from the users' point of view as the preceding SATA-II hardware and software did (and do).

The key to getting up and running quickly on the SATA-6G is to understand the functionality of the SATA-II and how to efficiently use it, either by studying the SATA-II product documentation for the first time, or reviewing the SATA-II documentation, or as a result of experience gained by prior or current use of the SATA-II hardware and software.

1.1.2 Front-panel SMA Connectors

The front-panel SMA connector pair present on the left side of the SATA-6G (as seen when facing the unit) can accept a (pair of) input signal(s), such as for use in Frame Error Rate (FER) test applications. These SMA connectors perform only signal input into the unit.

The front-panel SMA connector pair on the right side of the SATA-6G (as seen when facing the unit) can output a (pair of) signal(s), as may be useful in FER test or other applications. These SMA connectors perform only signal output from the unit.

Note that the SATA-II does not have similar SMA connectors on its front panel.

1.1.3 Downloadable Files

Refer to www.c-h-s.com/SATA-6G.shtml for SATA-6G-related downloadable files.

The SATA-6G.UsbDrivers.zip file has USB drivers files that Windows can be pointed to when the SATA-6G is connected for the first time.

Figure 1.1 - SATA-6G front view

The SATA-6G Control Application ZIP file, when downloaded, should be placed in a folder and unZIPped. The application is started by executing (double-clicking on) the EXE file. Note that when the SATA-6G unit is first powered on, it is not functional until the front-panel LED has finished blinking (as described previously). Therefore, the control application should not be started until that point, as the application will report an error if the unit is not then currently functional. Note that such an error may be reported when starting the application even when the unit is thought to be already functional. In such a situation, simply try restarting the application once again, possibly waiting a few seconds before doing so.

The SATA-6G firmware ZIP file, when downloaded, should be placed in the Control Application folder. A copy of the file should be made there and renamed with additional characters appended in the filename to indicate the firmware version number (as indicated on the download webpage). Note that the firmware file will not be used unless a firmware update has been started through use of the SATA-6G Control Application.

1.1.4 USB Hardware Interface

As the USB interface circuitry on the SATA-6G is powered by the USB connection itself, the SATA-6G does not have to be powered (that is, its external power supply can be left unconnected) in order for it (that is, its USB interface) to be recognized by Windows. Therefore, by just connecting the USB cable, you should be able to have Windows see the unit and ask for the USB drivers. Note that the front panel LED will be off regardless of whether a USB connection exists or not, if the external power supply is not connected. Note also that it is acceptable to leave things in that state for some period of time; however it is suggested that if the unit is not to be used for a lengthy period of time that the USB connection be removed, in addition to the external power being removed.

The SATA-II USB interface by way of contrast was powered only when the SATA-II was powered by its external power supply.

Figure 1.1 - SATA-6G back view

1.1.5 Expected LED Behavior

Connecting the unit to the external power supply and connecting the power supply to AC power, should result in the front-panel LED immediately showing yellow, and then flashing yellow/green a few times. The flashing should occur about 15 seconds after the unit receives power, indicating that the internal firmware load took place normally. At that point, the LED will be yellow when no active USB connection exists, and green for an active USB connection (assuming the USB drivers have already been loaded). Note that the LED will show green steadily only if the unit's USB cable is plugged in to a USB host (possibly via one or more intermediary USB hubs) and if/when the SATA-6G USB drivers have been loaded onto the Windows system.

If the normal firmware image fails to load for some reason, the LED will not flash after the first 15 seconds. Loading of the fallback image of firmware will then be attempted, which will result in the LED flashing (if the load succeeds) after about 30-45 seconds after power was first applied. If no LED flashing is seen to occur after about a minute or so, then none of the firmware load attempts succeeded, and no LED flashing will then occur (including no follow-on steady-green LED display). In such a situation, the unit's power can be removed and reapplied, with the firmware-load process then being reattempted.

1.1.6 CtrlApp Differences

Here is an overview to the more important differences between the SATA-6G Control Application (CtrlApp) and the SATA-II application:

1.1.6.1 Monitor Window -

The **Monitor** selection of the **View** pulldown menu currently does nothing.

1.1.6.2 Trigger Out Window -

On the Trigger Out window (accessed via the **View** pulldown menu), the **Toggle all Trigger Outputs** control has been added, which causes all four trigger outputs (regardless of which output has been selected in **Trigger Out** at the top of the window) to each toggle at a different frequency, the intended use for which is a quick check to verify all trigger outputs as being functional.

Note that the trigger outputs produce 1.5V nominal output high levels when connected to an unterminated 50-Ohm SMA or BNC cable, and produce 0.75V nominal output high levels when connected to a 50-Ohm terminated cable; these high-level voltages are basically 50% of that produced by the SATA-II. (The low output levels are nominally 0V in all cases.)

1.1.6.3 Main Window -

1.1.6.3.1 Save/restore of CtrlApp state --

On the main CtrlApp window, support is still provided for saving the "system state" to and restoring it from a file, named SATA-6G.SaveFile.txt; no support is however provided for saving to or restoring from non-volatile memory (NVRAM) in the hardware (as is the case with the SATA-II).

Additionally, reading from and writing to SATA-6G.SaveFile.txt occurs only when Read configuration from save file or Write configuration to save file are clicked on. When the CtrlApp starts up, instead of automatically reading the SATA-6G.SaveFile.txt file, another file, named SATA-6G.AutoSaveFile.txt, is read, and when the application is exited, the then-current configuration information is automatically written to that file. Note that the format of the two files is the same, so therefore they can be copied one to the other if the need arises. It is suggested that a copy of each of the two files be made in the folder with having the CtrlApp, so that it will be easy to restore either file if the files are ever corrupted. It is recommended that occasionally, as the application is used and the GUI and hardware configuration is possibly changed, that additional copies be made of the then-current versions of the files.

Note that the CtrlApp ZIP file downloadable from the CHS website contains not only the application EXE file, but "starter" SATA-6G.SaveFile.txt and SATA-6G.AutoSaveFile.txt files as well. When downloading the ZIP file containing a new CtrlApp version, there is typically no need to replace the existing TXT save files on your Windows system with the TXT files present in the ZIP file. Retaining the previously-in-use TXT save files should allow for a smooth transition from the previous version of CtrlApp to the new CtrlApp version.

1.1.6.3.2 Middle-column controls --

The function of many of the controls present in the middle column of the main window are self-explanatory and/or have not changed from the SATA-II version.

The CtrlApp **Host data source** set of controls affects where the "host" data to be examined is obtained from. With SATA1 selected, the host data is obtained from the H1 (leftmost) SATA connector. With SATA2 selected, the host data is obtained from the H2 (right-side) SATA connector. With SMA input pair selected, the host data is obtained from the left-side SMA connector pair.

Similarly, the CtrlApp **Device data source** set of controls affects where the "device" data to be examined is obtained from. With SATA1 selected, the device data is obtained from the D1 (left-side) SATA connector. With SATA2 selected, the device data is obtained from the D2 (rightmost) SATA connector. With SMA input pair selected, the device data is obtained from the left-side SMA connector pair.

1.1.6.3.3 Front-panel SATA connector signal buffering --

Any host-produced data present and coming in via the Host SATA1 connector is always buffered through and output to any device that may be connected to the Device SATA1 connector. Similarly, any device-produced data present and coming in via the Device SATA1 connector is always buffered through and output to any host that may be connected to the Host SATA1 connector.

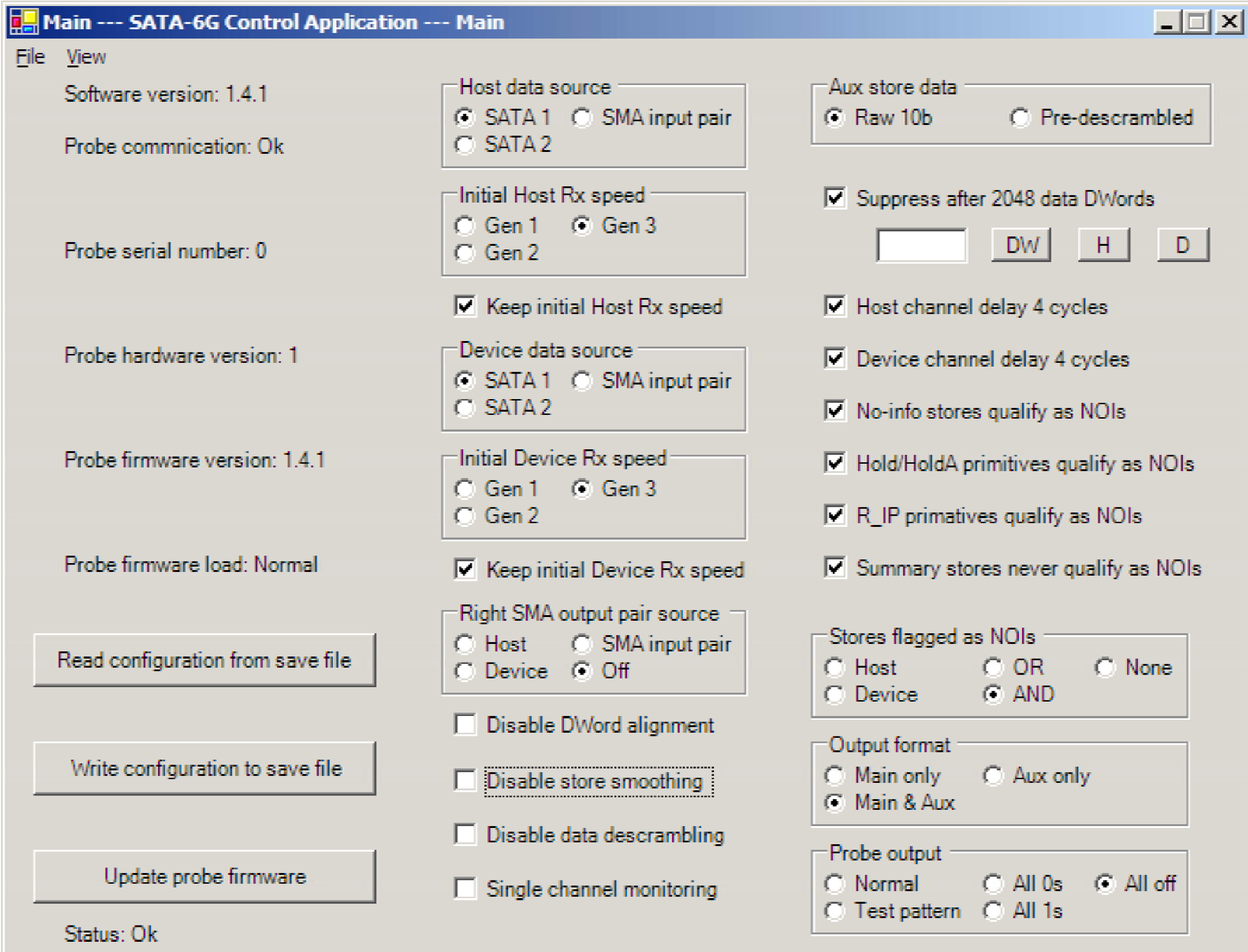

Figure 1.3 - SATA-6G Control Application Main window

The same holds true for the SATA2 Host and Device connectors and the through-buffering that always takes place for those connectors.

Note that unlike the SATA-II, through-buffering does not occur until the unit is powered and the CtrlApp has been invoked for the first time. (For the SATA-II, just powering on the unit generally sufficed to have through-buffering be active.)

1.1.6.3.4 Controls' effects upon signaling --

Changes to certain CtrlApp main window controls result in the hardware configuration possibly being reset, resulting in through-buffering possibly being momentarily interfered with. As this can result in disruption of signaling between host and device, it is generally recommended to refrain from changing CtrlApp GUI settings (at least the relevant ones) while SATA communication is occurring, and waiting until SATA signaling has terminated (when both host and device are producing squelch (or are powered off)) before changing CtrlApp controls' settings.

1.1.6.3.5 Controls affecting front-panel SMA output connectors --

The **Right SMA output pair source** set of controls affects what output occurs at the output SMA pair of connectors. When no SMA output is needed or being used, the selection of **Off** should be made.

For the **SMA input pair** selection, the SMA output pair outputs a copy of the SMA input pair input signaling. For the **Host** selection, a copy of the host signaling present at either the SATA1 or SATA2 connector is output, per whether the **Host data source** control selection is SATA1 or SATA2 (and, for **Host data source** set to **SMA input pair**, the host signaling copied is that of the SATA1 connector).

For the **Device** selection, a copy of the device signaling present at either the SATA1 or SATA2 connector is output, per whether the **Device data source** control selection is SATA1 or SATA2 (and, for **Device data source** set to SMA input pair, the device signaling copied is that of the SATA1 connector).

1.1.6.3.6 Probe output control --

For FER applications it is recommended that the **Probe output** control be set to the **All off** selection.

1.1.7 Pre-production Units

SATA-6G units which were shipped as late as Q2/2010 are considered pre-production units, with the case front and back faceplates' possibly having preliminary-version machining and printing.

1.2 INFORMATION RELEVANT ONLY FOR TLA PROTOCOL ANALYSIS

1.2.1 Logic Analyzer Probe Connections

1.2.1.1 Probe Requirements -

The Tektronix logic analyzer requires P6860 probes (having black clip-on elastomer holders (for use with "thick" printed circuit boards (PCBs))), 136 channels and 300MHz state acquisition. With regard to the last point, note that it may be necessary on the TLA Setup window to specify a higher-than-default clocking rate for the acquisition module (e.g., the default maximum clocking rate for some acquisition modules is only 235 MHz).

1.2.1.2 Probe Connection & Disconnection -

It is important to note that when the TLA probes are being connected or disconnected, the unit should be powered off. Additionally, all connections (other than the TLA probes themselves) should be physically removed (disconnected) from the unit, including the USB connection and any and all front- and back-panel SATA and SMA connections, to be maximally certain of protecting the SATA-6G. It is possible that the internal circuitry of the SATA-6G (the circuitry associated with the probe outputs) can be irreparably damaged if the TLA probes are not reasonably mechanically secure when other connections are made and the unit's power is applied.

Note that the CtrlApp main window **Probe output** group of controls has a selection of **All off**, which should ideally be selected when the TLA outputs are not being used (e.g., when the SATA-6G is not connected to or is not being used with a logic analyzer (as for FER testing). Additionally, the **All off** selection should be used if it is greatly inconvenient to unpower the unit and disconnect all other connections when connecting or disconnecting the TLA probes.

The preferred procedure, however, is that power be removed from the unit and all other cables be completely disconnected before connecting or disconnecting the TLA probes.

To reiterate:

> **It is critical that the logic analyzer probes be connected and disconnected from the SATA-6G only when the unit is NOT powered on, with all other cables completely disconnected from the unit.**

1.2.1.3 Probe Contact Area Cleaning -

It is recommended that the TLA probe-mating areas on the unit's PCB inside the case be cleaned (e.g., with a lint-free alcohol swab) prior to connecting the TLA probes. Note that the TLA probes themselves, including the clip-on elastomer holders etc., should NOT be cleaned with alcohol; refer to file ElastomerRequirements.pdf (Tektronix document #061-4254-01), which has been appended to the end of this document, and which outlines the Tektronix-recommended care and cleaning of the elastomer probes.

1.2.1.4 Probe Removal -

It is recommended when removing the probes (which again must be done with power removed from the unit or under a **Probe output** selection of **All off**), to watch for probes which may be difficult to readily remove due to the plastic guide pin possibly binding in the mating hole on the PCB. If this happens, rotating the probe back and forth gently until it becomes free, prior to lifting upward, may work well.

It is recommended when removing the TLA probes, to check the probes to ensure that one or more of the elastomer segments have not been left behind on the PCB (which has been known to happen). If a probe shows missing elastomer segment(s), it is suggested that the clip-on holder be replaced with a new holder having new segments. If elastomer segments are missing, it is important to then check the probe areas on the PCB inside the SATA-6G case, and see if any segments are present there. Any left-on-the-PCB segments need to be carefully removed (use of a tweezers may be required), and care needs to be taken to avoid letting any such segments roam freely inside the SATA-6G case if they become dislodged. Obviously, SATA-6G power should not be applied while any elastomer segments are sitting on the PCB or are possibly hiding inside the SATA-6G case somewhere.

1.2.1.5 Case Considerations -

1.2.1.5.1 Probe access openings --

The case has openings in its top to allow access for the P6860 TLA probes. The case has metal plates (inserts) for covering the openings. Units are shipped with the inserts taped into position in the case top, else (for those units which have been ordered with only the TLA analysis option) with the case top openings left open (with the inserts also provided, but not inserted into the case top).

If connection of TLA probes is required, the case top openings must be open. If the unit was shipped with the inserts in place in the case top, the inserts must first be removed. This can be accomplished through the use of a small-size flat-bladed screwdriver, which can be inserted into the slot at the side of the insert, and which can be used to pry the insert up and out from the case top. Note that the inserts are taped in place on the inside surface of the case top, and may be found to be somewhat difficult to dislodge. Slow, steady pressure is recommended when freeing the inserts. Note that the metal of the extruded aluminum case is relatively soft, so that the edge of the opening in the case top may wind up becoming marred to some extent in the process of using the screwdriver.

1.2.1.5.2 Use with no probes and case open --

When the unit is being used and the TLA probes are not connected (e.g., possibly for FER testing), it is acceptable to keep the case top openings open (e.g., if the inserts were previously removed), which will facilitate to an extent outbound convection airflow cooling of the unit. Alternatively, it may be desirable and it is acceptable to close or block the case top openings, in which case outbound airflow can still occur via other orifices in the unit, as well as via the internal blower (fan) whose exhaust port is located at the back faceplate of the unit.

With the case top openings open, care must be taken to prevent foreign objects from winding up inside the case, including particularly conductive objects which could obvious wreak havoc with the unit's circuitry.

1.2.1.5.3 Protection when not in use --

When the unit is not in use, and especially when TLA probes are not connected, it is important to keep the unit covered to protect it from dust and other foreign materials entering the inside of the case. Placing the unit is an appropriate bag (such as the antistatic bag in which it was shipped) would suffice. (There is no need to attempt to put the metal inserts back into place, which may prove difficult.)

1.2.1.6 Verification Of Probe Connections -

Verification of proper connection of the TLA probes is absolutely critical if reliable protocol analysis is to be performed. As with the SATA-II, the CtrlApp can be used to set the unit to produce test pattern data for output to the TLA probes, including all-0s, all-1s and a walking-bit pattern. It is important to verify that an acquisition of the test pattern data is able to be performed properly, as confirmed by the disassembler (set to the appropriate pattern-checking mode), before proceeding to use the unit for normal SATA acquisitions. This verification should be done when the probes are first connected, and also periodically thereafter (e.g., several times a week at a minimum), including especially when first using the unit after it has been idle for an extended period of time (even with the probes having been left connected).

Additionally, it is helpful to make use of the "Probes" display (in some TLA system software versions this is accessible via the Probes button on the Setup window; in other versions the activity of each channel is visible in the Setup window itself), which shows the real-time behavior of all of the TLA probes. The Probes display should be used before attempting the test pattern acquisitions just mentioned, in order to confirm that the probe connections appear generally to be proper and functional. The Probes display should also be used even before that when first connecting and tightening the probes, to ensure that proper electrical connection is being made without the probes being held in place too loosely or too tightly, either of which can result in problems with the logic analyzer acquiring data from the SATA-6G unit.

The recommend probe-connection-verification procedure is outlined immediately below.

1.2.1.6.1 Power off, cables and TLA probes disconnected --

Ensure that the unit power is off, with all cables and other connections to the SATA-6G removed, as outlined above.

1.2.1.6.2 Attach TLA probes --

Attach all probes and make all probe screws roughly finger tight, so that the probes are secured and not able to "go anywhere"; the probes should not be loose to any great extent. Note as discussed in Section 1.2.1.2 above:

> **It is critical that the logic analyzer probes be connected and disconnected from the SATA-6G only when the unit is <u>NOT</u> powered on, with all other cables completely disconnected from the unit.**

1.2.1.6.3 Apply power --

Apply SATA-6G power; verify proper SATA-6G front-panel LED behavior (as noted above).

1.2.1.6.4 Connect USB cable --

Connect the USB cable; verify that the LED then shows green (assuming USB drivers have previously been loaded, which should be the case).

1.2.1.6.5 Start CtrlApp --

Invoke the SATA-6G control application (which can be run on the TLA itself, or on some other Windows system).

1.2.1.6.6 Set <u>Probe output</u> to <u>All off</u> --

In the CtrlApp set the **<u>Probe output</u>** control to **<u>All off</u>**. Observe on the Probes display of the TLA the real-time state of all 136 probe channels; all channels should show low. Note that probe channels which are not making proper contact at the SATA-6G PCB will show low by default.

1.2.1.6.7 Set <u>Probe output</u> to <u>All 0s</u> --

Change the **<u>Probe output</u>** control on the CtrlApp window to All 0s. Observe the state of the TLA probes on the Probes display; all channels should still show low except for CK3 (which is the clock signal produced by the unit for use by the acquisition module), which should show activity (e.g., a double-ended vertical arrow (in some TLA system software versions)).

1.2.1.6.8 Set <u>Probe output</u> to <u>All 1s</u> --

Change the **<u>Probe output</u>** control on the CtrlApp window to **<u>All 1s</u>**. Observe on the Probes display that CK3 still shows toggle behavior. All other channels should now show high. Channels showing low, or which may be making some sort of intermediate connection and which therefore show toggling behavior, are not reporting a constant high and will need corrective action, as discussed below.

1.2.1.6.8.1 Check all probes ---

Per the Probes display, iterate though the each of the probes and tighten or loosen each of the two screws in turn which hold each probe. Observe that (over) tightening of the screws does not necessarily result in proper or better results. It is suggested that even probes whose channels appear to be working properly be checked, so as to determine the optimal mechanical range of tightness for the particular probe. For all apparently-working probes, apply a slight amount of pressure parallel to the surface of the SATA-6G unit to wiggle the probe slightly back and forth; verify that this slight mechanical stressing of the probe does not affect the Probes display results.

1.2.1.6.8.2 Probe corrective action ---

The following procedure is recommended in the case of a probe that cannot be made to show the expected probe behavior.

- Check that the probe being tightened and loosened is in fact the probe you think it is (trace the cable back to the acquisition module), and verify that it is located in the proper place on the SATA-6G unit (refer to probe placement information below).
- With the power to the SATA-6G unit off, remove the probe and check for missing elastomer segments, and segments left behind on the PCB in the SATA-6G unit.
- (Re)clean the area on the PCB (using alcohol and a lint-free cloth or swab.), and (re)clean the probe (NOT using alcohol). It may be necessary to remove the neighboring companion probe as well, to get the needed access to the area on the PCB.
- Put the probe(s) back in place, finger-tighten the screws, power the unit on, and again adjust the screw tightness while monitoring the Probes display.
- Consider replacing the elastomer clip-on holder (including the elastomer segments) in problematic cases. Consider swapping probe connections at the acquisition module and correspondingly at the SATA-6G unit, in more-problematic situations. Consider replacing the probe assembly in even more-problematic situations.
- Iterate as necessary.

1.2.1.6.9 Set <u>Probe output</u> to <u>Test pattern</u> --

Once the all-1s output pattern is properly indicated in the Probes display (except for CK3), change the **<u>Probe output</u>** control to **<u>Test pattern</u>**. Now, not only CK3, but all other probes as well, should show signal toggling behavior on the Probes display. If the all-1s output pattern worked, the test output pattern should also be found to work, although it is in fact a somewhat more demanding test situation.

1.2.1.6.10 TLA acquisition of test pattern --

Once the Probes display shows that proper probe behavior results for the all-0s, all-1s and test pattern outputs, then a TLA acquisition should be made of (at least) the test pattern output. The procedure that may be followed is:

- Ensure that in the CtrlApp main window **Probe output** is set to **Test pattern**; ensure also that **Output Format** is set to **Main & Aux**.
- On the Setup window make sure that the clocking selected is **Custom** or **SATA6GA** (and not synchronous, asynchronous, external or internal, etc.). Set **Format /Store Types** to **Main & Aux / Main & Aux**; also set **Acquisition** to **All**. As noted above, set **Speed / Max Clock Rate** to allow for 300 MHz acquisition.
- On the Trigger window ensure that a default trigger (trigger immediately) is set up.
- In the Listing window, right-click and select **Properties**; on the Disassembly tab under SATA6GA Controls scroll to the end of the list and set **Test Pattern Format** to **Main and Aux**, and set **Test Pattern Verification** to **Enabled: nominal** (assuming the CtrlApp **Probe output** control is set to **Test pattern**). Then click OK to dismiss the Properties window.
- Click on the **Run** button to perform an acquisition. Review the disassembly display to ensure that no acquired samples are flagged as being in error. It is suggested that the successful acquisition be saved to (.TLA) file, which file can be loaded later when needed to allow the test pattern acquisition to be quickly setup and performed again. Note that included in the example TLA acquisitions files downloadable from the CHS website, are example "good" all-0s, all-1s and test pattern acquisitions.
- Iterate as necessary; if improper acquisition results are obtained, return to using the real-time probes' signal display information to diagnose which probes are the problem, and to verify that the probe connection or functionality issues have been resolved. Once the Probes display shows good results, the test pattern acquisition should be able to confirm that situation, and no further iterations should usually be required.

1.2.1.6.11 Quick setup of the TLA for test pattern acquisition & verification --

In practice, the easiest and quickest way to configure the TLA to perform a test pattern acquisition (or a normal acquisition) is to load in an already-saved test pattern (or normal) acquisition (.TLA) file. At that point, once the CtrlApp controls are setup properly, the acquisition can be made, and the results checked; if the results are good then some other (normal) saved acquisition file can be reloaded and used to perform other (normal) acquisitions.

1.2.1.6.12 Mini-verifications are recommended --

Although reverification of proper test pattern acquisition should be done periodically as noted above, it is suggested (and also easy) to make mini-verifications from time to time simply by changing the Probe output control to Test pattern and viewing the real-time probe activity. This can be done in just a few seconds, and disturbs in no way the setup of any of the TLA windows (as performing a test pattern acquisition would). Such mini-verifications should be done as a matter of habit from time to time, as they are the only quick and simple way to have any reasonable degree of assurance that the probe connections are (still) valid and have not electrically degraded over time since the probes were last mechanically tightened into place.

1.2.1.6.13 Mini-verifications are insufficient --

While the Probes display is so handy that its use is essentially a requirement, by itself it is not sufficient; successful test pattern acquisitions must be done (at least initially, and possibly afterwards occasionally) in order to verify that all signal connections and timing are in fact (still) proper.

1.2.1.7 Probe Connection Diagram -

The following diagram indicates where each TLA probe should be connected on the SATA-6G unit, as seen when looking down on the top of the SATA-6G, with the front of the unit (where the four SATA connectors are located) to the left, and the back of the unit to the right.

Note as discussed in Section 1.2.1.2 above:

> **It is critical that the logic analyzer probes be connected and disconnected from the SATA-6G only when the unit is <u>NOT</u> powered on, with all other cables completely disconnected from the unit.**

```
         A2/A3.
         D2/D3.
                   D0  A0
                   D1  A1
                    .   .
(front)                          (back)
                   C0  C2
                   C1  C3
                    .   .
         E2/E3.
         E0/E1.
```

To reiterate:

> **It is critical that the logic analyzer probes be connected and disconnected from the SATA-6G only when the unit is <u>NOT</u> powered on, with all other cables completely disconnected from the unit.**

Note that the probes are to be aligned so that the probe's plastic guide pin is to be toward the right (back) or toward the bottom, as indicated by the eight "." in the diagram.

Note that if the wrong probes are placed in the wrong positions (albeit mechanically properly secured, let's assume), the error can be caught when a test pattern acquisition is done. Use of the Probes display can typically not catch such situations.

Note also that if the validity of the CK3 (clock) signal has been compromised, no acquisition may take place at all; a working CK3 channel is required for proper synchronous acquisition of test pattern (or normal) acquisition data. Useful test pattern information may still be obtainable however in such situations for the other channels, by changing to asynchronous (or internal) acquisition timing. In such a case (e.g., with samples taken every 2ns), the disassembler will report numerous errors (since not just one, but multiple samples are taken of each test pattern value, including completely-bad intermediate values occurring when the signals change state), but the disassembly display can nevertheless be studied to reveal which channels (other than CK3) may be functioning properly (or improperly). (Use of the Probes display is probably to be preferred in such situations however.)

Note that the order of display of the probe channels as seen in Figure 2.1 of the SATA-II Users' Manual, and as described in Section 2.2.5.3 there, is the same order as utilized and displayed in the case of the SATA-6G.

1.2.2 Disassembler Considerations

1.2.2.1 Disassembler File -

The SATA6GA Disassembler ZIP file, when downloaded, should be placed in a folder and unZIPped. The disassembler (and related files) are installed (either on the TLA, or on a Windows system having the TLA application) by executing the setup.exe file.

1.2.2.2 Clocking Acquisition Options -

On the Setup window the clocking (acquisition) options selections under **Format /Store Types** relating to Gen1@75MHz, which were relevant for the SATA-II (refer to Section 3.3.4.1 in the SATA-II Users' Manual), are not present for the SATA6GA disassembler.

1.2.2.3 Default Values Of Numeric Disassembler Display Controls -

As with the SATA-II, and as noted at the beginning of this document, when using the disassembler (for normal acquisitions), it is important to verify that the two numeric-value Disassembly display controls (Maximum Num Data and Max Data Display Lines) do not have values of 0 (unless you really want that, which would be seldom), since that would result in apparently-improper display results. It is possible that the two control values, which are supposed to be initialized to their maximum values, are initialized instead to 0 when Load Support Package is done to setup the acquisition module initially. (Note that the values of the controls have no effect upon test pattern acquisition displays.) The best work-around, once the control values are set e.g. to all-9s, is to save the TLA file, and then use that file when later acquisitions are done. That is, it is suggested to rarely if ever use Load Support Package, and instead leverage off previously-saved files and acquisitions.

1.2.3 Information Stores

1.2.3.1 Information Store Format Changes -

The SATA-6G produces stores for acquisition by the TLA having a slightly different format than those produced by the SATA-II (as documented in the SATA-II Users' Manual in Tables 7.1 through 7.5, and in Section 7 generally), as now explained in more detail.

1.2.3.1.1 Speed --

One set of changes relate to support for specifying the then-current speed of the host and device data (actually, the speeds at which the SATA-6G reception circuitry is then operating at to receive in the host and device data, which speeds would usually track the actual signaling datarates). Two bits in the Main store which for SATA-II had been used for relatively unimportant purposes have been redefined so that two host-speed and two device-speed bits of information are provided in each Main store. Specifically, for SATA-II, as seen in the Tables cited above:

E2(4) = DeviceRunningDisparityErrEnb
E0(1) = DeviceSpeed (0 -> Gen 1; 1 -> Gen2)
E0(0) = HostSpeed (0 -> Gen 1; 1 -> Gen2)
D1(2) = HostRunningDisparityErrEnb

In the case of SATA-6G:

E2(4) = HostSpeed(1)
E0(1) = HostSpeed(0)
E0(0) = DeviceSpeed(1)
D1(2) = DeviceSpeed(0)

The SATA-6G speed encoding is:

00 = Gen1
01 = Gen2
1X = Gen3

1.2.3.1.2 DecodedChar --

The information communicated via DeviceDecodedCharA-D (refer to Section 7.1.3) and HostDecodedCharA-D now expresses the speed as a two-bit value (encoded as noted above). Note in a related matter that the SATA-6G does not provide an indication of PHY locking, so the lock-related bits in DeviceDecodedCharA-D and HostDecodedCharA-D, which are present for SATA-II, should be ignored.

1.2.3.1.3 RegionDuration --

A further store format change is that a given value of RegionDuration (refer to Table 7.12) now represents twice the duration time duration compared with SATA-II.

1.2.3.2 Channel Groups & Symbol Tables -

As a result of the TLA output store format changes, the definition of channel group MSpeed has been changed accordingly (relative to SATA-II) in the SATA6GA disassembler-related files, along with the MSpeed symbol table. Additionally, the MDRDErrEnb and MHRDErrEnb channel groups have been removed. Also, the MDataHex, MDataDxxy, A10bDataHex and A10bDataDxxy symbol tables have been changed. The MOOBDuration symbol table has also been changed.

Note that the changes to the TLA store formats, the channel group definitions and the symbol tables, should make little or no difference in practice with regard to how most TLA trigger programs are formulated, e.g. as outlined in Section 6 of the SATA-II Users' Manual, and are (of course) a complete non-issue for FER applications.

1.2.3.3 Rate Of Information Store Production -

For SATA-II, the maximum rate at which TLA stores could be produced was 150 MHz, which allowed for a Main and an Aux store to be output per each Gen2 DWord (4 characters (32/40 bits)) occurring. For SATA-6G, the rate at which TLA stores are produced is 300 MHz, which allows for a Main and an Aux store to be output per each Gen3 DWord.

As with SATA-II, the rate of output store production is actually 0.1% higher than the nominal maximum DWord rate; the TLA store output rate is thus actually 300.3 MHz. This allows all SATA signaling, including Align primitives, to be received in, processed, and communicated to the TLA.

As with the SATA-II, since the TLA store rate is higher than the highest-expected Gen3 line rate, there is no new information available to be presented for one store in about every 1000, in which case a "No Info" store is produced. (Refer to the SATA-II documentation for further information regarding No Info stores.) As is the case with SATA-II, when receiving in signaling rates lower than Gen3, many of the TLA stores produced are No Info stores, with about 50% of the stores being No Info stores for Gen2 reception, and about 75% of the stores being No Info stores for Gen1 reception. The TLA acquisition module can readily be configured to not acquire No Info stores (refer to Section 3.3 generally). Note that the "store smoothing" functionality acts to coordinate the time of occurrence of the no-information conditions as recorded for the host and device datastreams, to maximize the information communicated in every TLA store. Note further that the disassembler Listing window controls can quite easily suppress display of any acquired No Info stores in a host or device acquisition display.

Note that this abbreviated discussion of No-Info stores has glossed over some important issues; it is recommended that the SATA-II documentation be referred to for more-complete information.

1.2.3.4 Store Smoothing -

The 0.1% frequency difference discussed just above results in 1 in every 1000 (approximately) acquisition clock cycles having no information to present to the acquisition module, which situation would be expected to result in acquisition of 999 (approximately) consecutive stores having data and one store having no data. Due to issues relating to synchronization of the serial datastream into the time domain of the acquisition clock, it is possible that yet additional consecutive no-info cycles can occur (although on the average the ratio of info to no-info would work out to 999:1 (approximately)); situations involving two (or even more) consecutive no-info cycles could be expected to be observed. The result of a number of consecutive no-info cycles would be that the relative time of occurrence of events in the host datastream relative to the device datastream would appear to "randomly" shift (although the presence of the no-info stores would indicate the reason for the time shift), in the data acquisition record and for the SATA-6G protocol analyzing logic, with user confusion or possibly even spurious errors (e.g., link-level errors) being reported.

In order to reduce or eliminate confusion or errors resulting from the occurrence of multiple consecutive no-info cycles, Ver 1.4.1 (and later) SATA-6G firmware implements new functionality which is enabled when store smoothing is enabled (i.e., when the CtrlApp **Disable store smoothing** GUI control is not checked (smoothing is enabled)). The new functionality acts to ensure that when a no-info condition occurs, another such condition will not occur for at least the next 15 acquisition clock cycles.)

Note that in the SATA-II, enabling store smoothing was possible only for Gen1 datastreams and not for Gen2 datastreams, since only the former had a significant number of no-info cycles; the store smoothing acted to arrange the timing of the two Gen1 datastreams so that generally both had no-info occurrences at the same time, with the result that most acquisition stores that were acquired would have useful Host and Device information.

If the same sort of functionality had been carried over into the SATA-6G from the SATA-II, then store smoothing would be functional in the SATA-6G only for Gen1 and Gen2 datastreams. Since however the SATA-6G also implements the new no-consecutive-no-info stores functionality mentioned above, which is controlled by the **Disable store smoothing** GUI control, it is the case for the SATA-6G that Gen3 data is also affected by the CtrlApp **Disable store smoothing** GUI control. In all cases, when the **Disable store smoothing** control is off, consecutive no-info situations cannot occur, and when the **Disable store smoothing** control is on, consecutive no-info situations can occur.

1.2.4 Datarate Specification & Tracking

Use of the SATA-II essentially required that the datarate(s) for the host and device (Gen1 or Gen2) be known up front and specified to the CtrlApp, as the algorithm provided for tracking speed changes was not particularly robust. The SATA-6G however uses a triple-redundancy technique to determine what datarate(s) are being used for the host and device signaling, by looking for Align primitives at each of the three possible datarates, and determining on that basis in an on-going manner whether the signaling happens at the moment to be at the 1.5Gb/s, 3Gb/s or 6Gb/s rate. When a squelch (no signal) condition exists, a specified initial speed is used to select the assumed initial datarate; once an Align primitive is seen, the datarate selection is updated. Note that this means that even when valid signaling is occurring following a squelch, the initial speed selection remains in force until an Align primitive is seen. Therefore for example, in the case of the host, even when D10.2 char production has started, and even once those characters are being received in properly by the analyzer, no change from the initial speed selection is made until the host eventually produces an Align primitive.

In a possible Gen3 scenario where the speed negotiation details are not of much interest, the initial speeds for both the host and device can be set to 6 Gb/s. However, the initial speed for the host and for the device can in fact be set independently. Therefore, in a Gen3 scenario where the speed negotiation details are of some interest, the initial speed for the device can be set to 6Gb/s, while the initial speed for the host can be set to 1.5 Gb/s; the reason for doing so would be to allow some of the D10,2 chars produced initially by the host to possibly be recorded. In general, the (only) reason for setting or changing the initial speed setting for the host or device is to obtain the benefit of being able to see data, if it is in fact occurring at the datarate expected, in advance of when the first Align primitive occurs. Note that it is also possible to fix the host or device speeds at the specified initial datarate, thereby defeating the auto-speed-selection mechanism.

Note that preliminary measurements indicate that once a squelch condition has ended or a change in the datarate has occurred, reliable data monitoring may be possible within less than a microsecond for a 6Gb/s datarate. This means that the amount of data lost (for analysis) in such situations may be only on the order of hundreds of DWords; this of course may or may not be critical, depending upon what is being communicated between host and device during that time period.

Note that the triple-redundancy monitoring technique mentioned above should not be confused with the SATA-6G optional ATM (All Traffic Monitoring) mode, for which there is essentially no downtime at all following squelch or datarate changes.

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